

**WMB (IMS) Monday 08:00 – 17:00 BCEC Room 157C**  
**Parameter Extraction Strategies for Compact Transistor Models**  
**Full-day workshop reviewed by MTT-1, IMS09**

**Organizer(s):**

Matthias Rudolph, Ferdinand-Braun-Institut, Germany; MTT-1, MTT-14, IMS TPC.  
David Root, Agilent Technologies, USA; MTT-1, IMS TPC.  
Christian Fager, Chalmers University, Göteborg, Sweden

“Transistor modeling” often means to circuit designers the determination of the model parameters in order to fit a selected model to a specific device. Parameter extraction and model verification are vital to make theoretically accurate device models practically useful. However, the modeling literature and model documentation usually focus primarily on how the device physics or phenomena are represented in a model, while the question of how the parameters can be determined is often only briefly addressed. It is the aim of this workshop to provide a broad overview of the different techniques and methods of parameter extraction. Rather than discussing individual models, generic strategies will be presented and real-life challenges will be addressed, like the impact of package, temperature and dispersion. It is the purpose of this workshop to provide a comprehensive introduction in order to enable the attendee to successfully deal with devices like GaAs & GaN HEMT, LDMOS, CMOS, GaAs & SiGe HBT.

**Speakers:**

1. Matthias Rudolph, Ferdinand-Braun-Institut für Höchstfrequenztechnik (FBH), Germany  
“Introduction to Transistor Model Parameter Extraction”

This introductory talk aims at providing an integral view on model parameter extraction. The questions to be addressed will be - how to characterize and verify model accuracy - definition of area of validity (“it depends on what you want”) - which device to choose? - what effects to expect? (extrinsic parameters, distributed effects in larger transistors, dispersion, thermal effects etc.) - model extraction routine workflow This talk therefore will put the details discussed in this Workshop later on in depth in a general perspective

2. Masaya Iwamoto, Agilent Technologies, Santa Rosa, CA, USA  
“DC and Thermal Modeling: III-V FETs and HBTs”

Topics relating to DC and thermal behavior of compound semiconductor transistors are presented, focusing on practical applications such as compact modeling, process development, and reliability. Typical DC characteristics of III-V bipolar and field-effect transistors are reviewed, and some examples of parameters that can be extracted from these relatively simple measurements are given. These parameters associated with the transistor in turn can be used for compact models and process development/monitoring. For high power and high speed devices, temperature variation due to power dissipation is significant, and self-heating effects must be taken accounted for accurately. Modeling topics such as thermal resistance extraction, thermal behavior of devices, and thermal simulations will be discussed. Finally, practical examples in the area of device reliability assessment are given where both DC parametric testing and thermal modeling are important.

3. Sonja Nedeljkovic, RFMD, Greensboro, NC, USA

“Extrinsic Parameter and Parasitic Elements in III-V HBT and HEMT Modeling”

This presentation discusses how to measure and account for the extrinsic parameters found in III-V HBT and HEMT models as well as the parasitic elements that arise in device scaling. It covers the common methods of extracting device extrinsic parameters, such as cold FET and open collector approaches, and includes test structures and de-embedding techniques. It also shows the parasitic elements introduced with device scaling and gives an approach of determining them with EM simulations. Lastly, it compares an acceptable approximations in dealing with the parasitic elements that aid in simulator operation.

4. Christian Fager, Chalmers University, Göteborg, Sweden

“Uncertainties in Small-Signal Equivalent Circuit Modeling”

This presentation will give a general view on the effects of various sources of uncertainty in the process of extracting transistor models. Different modeling examples will be presented to illustrate how uncertainties influence the extraction results. Based on these results, new extraction techniques will be introduced which utilize statistical methods to obtain more accurate extraction results. We will show how these techniques can be applied in de-embedding of high frequency on-wafer measurements. Finally, we will present a new method for identification of models with an optimized complexity vs. uncertainty trade-off.

5. David E. Root, Agilent Technologies, Santa Rosa, CA, USA

“The Large-Signal Model: Theoretical and Practical Considerations, Trade-offs, and Trends”

This presentation will concentrate on key requirements and trade-offs of the large-signal model formulation. Best practices are presented for formulating large-signal constitutive relations for well-defined models and robust convergence in nonlinear simulators. Relationships among small-signal quantities, such as current sources are reviewed for the traditional problem of constructing nonlinear models from DC and linear data. Methods comparing and contrasting integration with advanced recent methods using artificial neural networks are reviewed. Challenges and trends allowing more direct construction of nonlinear models from modern large-signal instrumentation such as nonlinear vector network analyzers are outlined. Alternatives to traditional “compact” large-signal models provided by recent advances in nonlinear behavioral modeling using X-parameters and similar approaches are summarized.

6. Jens Flucke, Ferdinand-Braun-Institut für Höchstfrequenztechnik (FBH), Germany

“Modelling of Large Packaged High-Power Transistors”

This talk provides a step-by-step tutorial on model parameter extraction for high power transistor packages. The extraction is performed on the basis of multiport em simulations and verified through measurement at the example of a packaged 30 W Power-GaN-HEMT. First, the effects observed in a package and their impact on the transistor performance are discussed in detail. The focus lies on mutual coupling of the bond wires and on current and field distribution on the

package leads and bond wires which is analyzed through 3D em simulation. Second, it will be shown how a suitable equivalent circuit is defined and how its parameters can unambiguously be determined from simulated Z-parameters. Finally, the performance of the full transistor model, consisting of the package description and the model for the transistor power bar will be presented and discussed.

7. R. Quéré, MITIC/XLIM University of Limoges, France

“Nonlinear Characterization and Modeling of Low Frequency Dispersive Effects in Power Transistors”

Low frequency dispersive effects are known to strongly impact the behavior of power amplifiers fed by complex modulated signals like pulsed in Radar Applications or phase and amplitude modulations in communications systems. They limit the RF performances of devices. Therefore it is of prime importance to characterize and model those effects in view of the circuit design improvement (better models) or in view of process technology improvement (better devices). The talk will present a number of characterization techniques like pulsed measurements, low frequency measurements, CW and pulsed frequency and time domain load pull measurements to assess the origin and the effects of low frequency dispersion in power transistors. Moreover an insight into the nonlinear behavior of trapping phenomena in GaN HEMT will be proposed through the aid of nonlinear LF-RF transistor modeling

8. Dominique Schreurs, KU Leuven, Belgium

“Optimizing (Non-)Linear Measurements for Model Construction and Validation”

Microwave device models are typically based on measurements as opposed to physical device simulations. The time needed to acquire the data often takes longer than the model construction itself. The presentation will focus on ways to render the characterization process more efficiently. Two cases will be presented. In terms of models based on linear measurements, the use of adaptive methods to collect the bias-dependent S-parameter data will be explained and discussed. In terms of models based on non-linear measurements, the impressive reduction in measurement time by using modulated –or multi-sine– excitations will be clarified. Finally, the optimal selection of non-linear measurements for model validation will be elaborated upon.

9. Pete Zampardi, Skyworks Solutions, Newbury Park, CA, USA

“Practical Statistical Simulation for Efficient Circuit Design”

All processes vary, some vary A LOT. This tutorial discusses an overall strategy for developing and implementing statistical models to design RF circuits in GaAs HBT technology. While the examples used are for developing handset power amplifiers, the principles apply to other devices and technologies (analogies for other technologies are discussed). Key features of this approach are: “unified” models where devices share parameters when constructed from the same physical process layers, using Design-of-Experiments to define the variations and minimize the required number of simulation runs, and a “device-up” approach, using basic device physics, to define the factors used in the experimental DOE runs to determine correlations among model parameters. This approach allows the enhancement of already existing models with a few simple

modifications. Specific examples of GaAs HBTs and GaAs MESFETs from a BiFET process will be presented.

10. Manfred Berroth, Universität Stuttgart, Germany  
“Noise Modeling”

Low noise amplifier as well as all kinds of oscillators suffer from noise generated by the active devices. Although the three most important types of transistors (MOSFET, HBT and HEMT) show significant differences in their noise characteristics, there are common noise sources and methods to characterize the noise of the devices at low and high frequencies. This part of the workshop will present the basic noise sources of transistors and high frequency equivalent circuit models are introduced for the three types of transistors and their noise properties are compared.