

WSD (RFIC) Sunday 08:00 – 17:00 BCEC Room 157C

Self-Interference and Co-Habitation Considerations in Complex SoC and SiP Integrated Solutions

Full-day workshop reviewed by RFIC.

Organizer(s):

Jan Niehof, NXP Semiconductors.

Oren Eytan Eliezer, Texas Instruments.

Paul Blount, Custom MMIC Design Services; RFIC TPC.

With the integration of RF, mixed signal and digital building blocks on a single die, combined with the trend of increased frequencies (both in the RF and in the digital circuitry), it is essential to consider various on-chip coupling effects in the early design phases of the RF SoC or SiP. Additionally, provisions should be made for mitigating the impact of peripheral interactions (e.g., package, antenna), as well as the potential for self-interference, such that these are either eliminated or can be resolved on the fabricated product without hardware redesign. The focus of this interactive workshop will be on resolving self-interference problems: on-chip coupling effects, chip-package co-design, substrate issues, coupling-aware RFIC floor planning, digitally assisted solutions for interference problems, design practices, modeling and CAD/EDA capabilities to address coupling effects. Recognized companies and partnerships active in the semiconductor industry will present actual issues encountered in their designs and the solutions/design-practices used to address them. Interactive discussions will be facilitated to exchange valuable ideas for the benefit of participants and the industry at large.

Speakers:

1. Jonathan Jensen, Intel

“Single Chip Radio Design; Thinking Beyond the Circuits and the Silicon”

Advanced single-chip wireless devices contain a higher level of integration than previous designs. Current radio solutions contain RF, analog and digital circuits; each operating semi-autonomously. The move to reduce cost and form-factor drives the integration of circuits that historically have been not been part of the silicon. The goal is to integrate RF, analog, power management and digital functions without impacting performance. The design of the communication system must be accomplished starting from the board level and continuing down through the package to the SoC silicon floor plan. Circuit functionality must be considered in the environment of the package and the board. Isolation structures and periphery require a high level methodology that starts at the board and works down into the silicon. This discussion will target a top down approach for single-chip radio design, which is demonstrated through two generations of single chip radio designs.

2. Stephane Bronckers, IMEC

“A Novel Methodology to Predict the Impact of Substrate Noise in Complex Analog/RF Systems”

Analog/RF circuits are prone to substrate noise coupling. When an analog/RF circuit is malfunctioning because of substrate noise coupling, the designer is often left without a clue of how to solve the problem. We propose a fast and easy-to-use methodology to predict the impact of substrate noise on large circuits. This methodology combines the strengths of three commercially available tools often used by analog designers namely: 1. an EM-simulator. 2. a parasitic extraction tool. 3. a circuit simulator. During this workshop, the designer learns how to set up the simulation environment for different silicon examples. The complexity of the examples varies from a single transistor up to a DC-to-5GHz wideband receiver. Finally, this workshop explores if 3D-stacking offers an opportunity to reduce the substrate noise coupling.

3. Scott Morris, RFMD

“Innovative Technique of Shielding for RF Applications at Package Level”

There are many different shielding technologies available for EMI shielding in Radio Frequency (RF) applications. We compare these different EMI shielding technologies and discuss an innovative way of providing EMI shielding at the package level. This novel concept provides improvements in form factor, ease of use and cost compared to traditional shielding approaches. A comparison is made between traditional board-level approaches like metal cans or lids and emerging package level technologies such as conductive paint, embedded shields and conformal plating. Electrical performance, manufacturability, and reliability between the different packaging technologies are also discussed. A thorough look at the advantages and limitations between these different EMI shielding technologies are also shown.

4. Matthias Locher, ST-Ericsson

“Bottom-up coexistence physical design and verification approach for multi standard SoC”

Today’s SoC’s contain multi standards that have to co-exist all at the same time. After best practices done on Top-down approach, there are still a couple of potential critical couplings that need to be controlled and verified on the physical level.

In this workshop we focus on digital noise analysis affecting the performance on RF systems, but also look into various simulations of coupling mechanisms and their effect in to the total system.

5. Nikos Haralabidis, Broadcom

“SoC System and Physical Design Approach for Co-Existence of Transceivers of Multiple Standards”

6. Oren Eliezer, Texas Instruments

“Software Assisted Radio Design to Compensate for Analog Impairments and for RF Interference Effects”

Transceiver SoC integration often involves not only the co-habitation of digital circuitry, mixed signal and sensitive RF blocks, but often even multiple transceivers. Although there is increased potential for interference amongst the integrated functions, there is also greater potential for coordination between them and for the implementation of means to mitigate the self-interference, as gate densities are increasing and processing power and memory can be made available within the SoC. This tutorial proposes a design-for-interference-mitigation (DfIM) approach that considers the potential for inevitable mechanisms of self-interference that could show up at the post-silicon stage, and addresses these through low-cost digital and software-based adaptive mechanisms, thus reducing the need or extent of changes in a hardware revision. Several examples will be presented, which are based on spectral spreading of clock signals, and on frequency/phase adjustment of aggressing signals.

7. José Luis González, Universitat Politecnica de Catalunya

“Substrate Noise Interference in RF Integrated Circuits”

Digitally originated switching noise is easily coupled, mainly through the substrate, to analog and RF circuitry integrated in the same silicon die. Once received by the RF section building-blocks it may perturb the normal operation of such circuits in various ways. In this talk, the main impact mechanisms for LNAs, Mixers and VCOs will be presented and discussed, as well as the consequences of this interference at the radio receiver or transmitter system level. Both analytical expressions and experimental examples are used to illustrate the main effects of substrate noise onto the various RF blocks. The main relations between circuit design parameters and substrate noise sensitivity will be presented.

8. Francois Clement, Coupling Wave Solutions

“Electrical Signal Integrity Analysis in Mixed-Signal and RF ICs”

With the dramatic increase in system complexity together with the lack of communication between IP authors, interfering noise is exploding the number of silicon failures. Consequently, existing design flow and methodology need to incorporate better understanding and solution to maximize system robustness within strong economic constraints. The lecture reviews the many aspects of interfering noise and focuses on cross-talk impact on RF blocks in advanced mixed-signal SOCs. Objective is to present a methodology to increase design robustness with respect to noise during IP authoring and integration in systems on chip (SOCs) and systems in package (SIPs). Injection mechanisms are reviewed and explained as well as transfer mechanisms through the combination of substrate, interconnects and package. Impact on sensitive IPs (high speed digital, analog and RF) is addressed. In parallel, state-of-the-art modelling and analysis software solution is presented.

9. Jan Niehof, NXP Semiconductors

“Dealing with Physical Design Issues in Complex RF Applications”

For RF and broadband applications it has become essential to co-design (as early in the design process as possible) the IC with its physical environment, such as to certify that the final packaged and mounted product meets the specifications. Also the impact of physical design aspects on system level behavior needs to be accounted for in the design and verification of mixed (RF, analog, digital) circuits. Modeling / simulation of physical phenomena is complex and difficult, and is always a matter of trade-offs (accuracy, speed, abstraction level). The presentation will focus on the key requirements to address physical design issues in the early design phases of complex RF design. Typical physical design issues encountered, such as on-chip coupling effects, chip-package/peripheral interaction, substrate coupling and co-habitation, will be discussed.