

WSG (RFIC) Sunday 08:00 – 17:00 BCEC Room 52A
Challenges for Future RF Integration
Full-day workshop reviewed by RFIC.

Organizer(s):

Gernot Hueber, DICE GmbH & Co KG.

R. Bogdan Staszewski, TU Delft.

Stefan Heinen, RWTH Aachen University; MTT-23, RFIC TPC.

Current and future transceivers for mobile terminals are facing increasing complexity because of the markets demands for more standards, lower cost, lower power consumption, and higher data-rate. As a result, multi-band and multi-mode radios covering the diversity of communication standards impart unique challenges on the RF-transceiver design due to limitations in terms of reconfigurable RF components that meet the demanding cellular performance criteria at costs that are attractive for mass market applications. The focus of this workshop will be on the challenges the cellular standards pose on future transceiver integration, along with a thorough discussion of advanced techniques for receivers and transmitters towards integration in a SoC. Approaches include novel architectures, highly configurable analog circuitry, digitally assisted and enhanced analog/RF modules and the integration of digital signal processing into the traditionally purely analog front-end. However, the utilization of digital signal processing capabilities is in line with the ongoing trend towards SoCs in minimum-feature-sized CMOS in the cellular market. Moreover, advances in the field of RF front-end modules and novel analog signal processing architectures are covered to give a consolidated outlook on future concepts for cellular radios.

Speakers:

1. Robert Bogdan Staszewski, TU Delft, The Netherlands
“Advances in Digital RF Architectures”

In the last few years, a series of breakthrough innovations have been made to transform analog-intensive RF circuitry into digitally-intensive implementations. In Texas Instruments, this disruptive technology falls under the umbrella of a Digital RF Processor (DRP) platform and enables to integrate almost all of cellular phone modem electronics into a single IC chip fabricated using nanoscale digital CMOS process. The first such single-chip mobile phone was sampled in December 2004 and is now in a mass- volume production targeting ultra low cost handsets for the Emerging Markets. As the Emerging Markets consumers get more sophisticated, there will be an increase in demand for more sophisticated phones with 3G modem interface, as well as wireless connectivity, such as Bluetooth, Wireless LAN, in addition to mobile digital TV and GPS. This presentation will overview recent advances in digital RF architectures in more sophisticated wireless standards beyond GSM and EDGE.

2. Bertan Bakkaloglu, Arizona State University, USA
“Reconfigurable Transmitters and Power Management”

In the first part of this presentation various RF power amplifier supply regulation schemes will be presented. These techniques enable the configurable transmit PA architectures. As CMOS technology is rapidly moving towards deep submicron gate lengths, supply voltages for analog, mixed signal and RF circuits are continuously decreasing. With the reduction of the supply voltage, noise, ripple and cross-coupling on the power supply line starts playing a dominant role in an RF transceiver SOC noise budget. Specifically, synthesizer phase noise, TCXO reference noise, LNA and mixer noise figure and audio performance are heavily influenced by the supply noise and ripple. In the second portion of this talk several power regulation strategies will be analyzed for reconfigurable RF transceivers.

3. Larry Larson, University of California, San Diego, USA
“Power Amplifier Integration Challenges for Highly Integrated Multi-Mode Transceivers”

This presentation describes power amplifier integration challenges for highly integrated multi-mode transceivers.

4. Aarno Pärssinen, Nokia Research Center, Helsinki, Finland
“RF System and Architecture Challenges for Multi-Standard Mobile Devices”

Mobile devices should provide a seamless access to new and quickly evolving internet services. High-speed packet based data traffic is ultimately the key driver in many of the applications and the role is rising when the transfer of high-quality video streams will become more common. At the same time many of the applications including for example voice, short message, location and some of the data synchronization services do not require the widest possible bandwidth. Hence, multi-standard radios are a must to fulfill all the consumer demands with minimum power consumption. This implies multitude of technology options to optimize the radio platform in different products. The emphasis to the lowest possible cost, large volumes and uniformity in the product design will not provide any easily solvable tradeoffs when flexibility to market trends must be achieved.

5. Yann Deval, IMS Laboratory, Talence Cedex, France
“Toward Software Radio Receiver”

The Software Radio (SR) receiver concept is claimed to be a solution toward low power, low cost reconfigurable systems. Indeed, characterized by a single chip solution SR receivers are able to handle any RF standards. Nowadays, though, SR receiver is still a dream as far as handsets are concerned, and Software Defined Radio (SDR) has been investigated by the RF community as an intermediate solution since technical bottlenecks will stay unsolved for, at least, the next 15 years. This talk focuses on the design of a

wide band, low power, and low cost analog signal processor, the Sampled Analog Signal Processor (SASP) chosen to interface the antenna and the ADC in a SR receiver chain.

6. Sebastian Hoyos, Texas A&M University, USA
“Multi-Path Receivers Architectures for Wideband Multi-Standard Radios”

This talk will present multi-path receivers architectures as a potential candidate for the design of software-defined receivers. These receivers parallelize the front-end by expanding the RF input signal. Each parallel path comprises of a switched gm-C filter structure that is modified to combine mixing with a base function, windowing and integration. Due to parallel digital signal processing, each path operates only on a fraction of the signal bandwidth, thus relaxing the tracking bandwidth requirements and minimizing the power consumption of each sampling path. Further, the lower speeds provide robustness to jitter in the sampling clocks, which otherwise can impose a major limitation in achieving high dynamic range. This topology enables the realization of a Software-defined radio multi-standard receiver that not only works for narrowband standards like GSM and Bluetooth, but also for wideband standards like Wimax and Wi-Fi and very wideband standards like ultrawideband.

7. Ranjit Gharpurey, University of Texas at Austin, USA
“Interference Cancellation and Linearity Enhancement in Wireless Receiver Front-ends”

Front-end linearity requirements arising from interferers can pose a major design challenge in transceivers for several commercial wireless systems. The increasing usage of spectrum, and consequent increase in the level and density of interferers, continues to further exacerbate the severity of the problem. This issue gains special significance in short channel CMOS implementations due to lowered supply voltages. In this presentation, we will explore circuit techniques and architectures that address the front-end linearity challenge. Design approaches including the use of on-chip filters and passive terminations, feedback, feedforward compensation of non-linear products, and the use of parallel receiver paths will be discussed. Practical examples will be presented and the impact of these techniques on dynamic-range, as well as specific linearity parameters will be considered.

8. Geoff Dawe, BitWave Semiconductor, Lowell, MA USA
“Software Defined (Configured) Radio Transceivers”

Multi Mode, Multi Standard applications are driving integration in handset and MID devices. In order to meet the aggressive cost objectives of these solutions, some amount of programmability in the RF transceiver is desirable. This programmability must be balanced against the strict signal performance and power consumption restrictions that are imposed. In this workshop, we will investigate the Softransceiver© approach to breaking the programmability performance paradox.