

**WSK (RFIC) Sunday 13:00 – 17:00 BCEC Room 156C**  
**Digitally Assisted Analog and RF Circuits**  
**Half-day workshop reviewed by RFIC.**

**Organizer(s):**

Joel L. Dawson, Massachusetts Institute of Technology.  
Stewart Taylor, Intel.  
Josie Ammer, Qualcomm.

The purpose of this workshop is to push forward the discipline of digitally assisted analog and RF design by taking a snapshot of the cutting-edge work going on in this field. Rather than hunt through the various journals and conference proceedings to piece together design trends, we offer attendees the chance to hear oral presentations from several of the leading experts in this young field. The workshop format is particularly advantageous for this topic, as in our view many of the breakthroughs in digitally assisted RF will find inspiration from similar work going on in analog design, and vice versa. Attendees will get a chance to hear about and ask questions concerning published work, and will also get a glimpse at cutting-edge but as-yet-unpublished work. Most importantly, attendees are encouraged to share their own thoughts and expertise concerning the techniques that are discussed. We expect the open exchange to benefit presenters and listeners alike.

**Speakers:**

1. Joel L. Dawson, Massachusetts Institute of Technology  
"Digitally Assisted Architectures for RF Transceivers"

This presentation focuses on the principles of good digitally assisted design, and examines a few recent successful architectures. Chief among the examples treated is a thorough analysis and characterization of a new power amplifier linearization architecture, with an exploration of its advantages and limitations. This architecture represents a new type of hybrid design for linearizers, in which functionality is optimally partitioned between the analog and digital domains. The idea centers on classic analog Cartesian feedback, using digital techniques to surmount the difficulties that have plagued Cartesian feedback in the past. Among these difficulties, perhaps the most severe is the need for high closed-loop bandwidth, which is impossible if a SAW filter is in the transmission path. Also discussed are a new technique for extremely low-offset multipliers, mixers, and VGAs, and a new architecture for medical implantable transceivers.

2. Boris Murmann, Stanford University  
"Overview of Digital Correction Techniques for High-Speed Data Converters"

Over the past several decades, a multitude of techniques that leverage digital logic to correct analog errors in ADCs and DACs have evolved. The purpose of this lecture is to provide an overview of these techniques for analog and RF circuit designers who are not necessarily experts in the field of data conversion. The presentation begins with a broad

introduction discussing foreground versus background schemes, and the distinction between static and dynamic errors. The core material will focus primarily on high-speed Nyquist ADCs, illustrating commonly used schemes used in flash, pipelined and successive approximation architectures. This lecture ends with a discussion on the latest trends in related research.

3. Larry Larson, University of California at San Diego  
"Digitally Enhanced RF Circuits"

This presentation provides an overview of digitally enhanced RF circuits and algorithms.

4. Khurram Muhammad, Texas Instruments  
"Software- Assisted Radio Design to Compensate for Analog Impairments and for Interference Effects"

The performance of the analog circuitry in current-generation CMOS SoCs suffers not only from natural process variations but often also from interference originating from analog and digital blocks sharing the same die. Additionally, aggressive production-cost targets prohibit costly testing that could identify marginally compliant devices, and do not allow for yield loss that would be attributed to excessive self-interference. However, modern CMOS SoCs can offer high-density digital gates and processing power at a low-cost, which enable sophisticated self-compensation and self-testing algorithms to be developed to address the design impairments and the potential self-interference problems. This tutorial presents several examples of digitally assisted design and of software based mechanisms that target performance optimization, self-interference mitigation and built-in-self testing in a cellular transceiver, thus allowing production-yield maximization and cost minimization.

5. Michael P. Anthony, Intersil Corporation  
"Mixed Digital/Analog Correction of Mismatch and Process Variability in a Pipeline ADC"

Trimming of analog circuits during test is a time-honored method of improving performance and yield by correcting for process variation and device mismatch. An alternative to trimming at test is adjustment by on-chip circuitry, either in foreground or background. On-chip correction requires a suitable stimulus, analog circuitry to perform the actual adjustment, analog and/or digital circuitry to detect the error to be corrected, and digital circuitry to control the process. In practical high-performance analog designs such added circuitry may represent a small fraction of total circuit area and power, and thus provide a substantial overall benefit. In some cases this mixed-mode approach, incorporating analog correction with digital detection, may be more area- and power-efficient than either analog "overdesign" or purely digital detection and correction. These concepts are illustrated using an interleaved pair of 12-bit 250-MSPS ADCs.